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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,544	09/24/2004	Wen-Kuo Chu	13529-US-PA	5543

31561 7590 04/18/2007  
JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE  
7 FLOOR-1, NO. 100  
ROOSEVELT ROAD, SECTION 2  
TAIPEI, 100  
TAIWAN

EXAMINER
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WON, BUMSUK

ART UNIT	PAPER NUMBER
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2879

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/18/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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**Office Action Summary****Application No.**

10/711,544

**Applicant(s)**

CHU ET AL.

**Examiner**

Bumsuk Won

**Art Unit**

2879

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --****Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 15 March 2007.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1,3-8,21 and 22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1, 3-8, 21, 22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_.

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### **DETAILED ACTION**

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/15/2007 has been entered.

#### ***Response to Amendment***

The amendment filed on 3/15/2007 has been entered.

#### ***Response to Arguments***

Applicant's arguments with respect to claims 1, 3-8, 21 and 22 have been considered but are moot in view of the new ground(s) of rejection.

#### ***Claim Objections***

Claims 1, 3-8, 21 and 22 are objected to because of the following informalities: In claim 1, "disconnected to each other" should be "disconnected from each other". Appropriate correction is required. Claims 3-8, 21 and 22 are objected to due to claim dependency.

#### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**Claims 1, 3- 5, 7, 8, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Urabe (2004/0090175) in view of Yuki (2005/0059185).**

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**Regarding claim 1**, Urabe discloses an active matrix OLED panel (figs 1-5) comprising: a pixel structure layer (bottom part of the panel) disposed on a substrate (1) wherein the pixel structure layer comprises an active device matrix (fig 5) and an anode pattern layer (A); an organic light emitting layer (10) disposed over the anode pattern layer wherein the organic layer comprises first, second, and third organic layers (RGB); and a cathode layer (12) disposed on the organic layer wherein the cathode layer comprises cathode patterns, first cathode pattern disposed on the first organic light emitting pattern, second cathode pattern disposed on the second organic light emitting pattern, third cathode pattern disposed on the third organic light emitting pattern (fig 4C), and the first, second, and the third cathode patterns are disconnected from each other (figs 3 and 4C).

Urabe does not disclose the first cathode pattern being electrically connected to a first voltage, the second pattern being electrically connected to a second voltage, and the third pattern being electrically connected to a third voltage, and the first, the second, and the third voltage are different from each other.

Yuki discloses an OLED device (figure 7) having first cathode pattern (R, red) being electrically connected to first voltage (701), second cathode pattern (G, green) being electrically connected to second voltage (702), third cathode pattern (B, blue) being electrically connected to third voltage (703), and the first, the second, and the third voltages are different from each other (figure 8), for the purpose of suppressing the luminance variance of each color independently (paragraph 153).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have first cathode pattern being electrically connected to first voltage, second pattern being electrically connected to second voltage, and third pattern being electrically connected to third voltage, and the first, the second, and the third voltage

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are different from each other as disclosed by Yuki in the panel disclosed by Urabe, for the purpose of suppressing the luminance variance of each color independently.

**Regarding claim 3,** Yuki discloses first, second, and third cathode lines (figure 7, 704, 705, 706) electrically connected to the first, the second, and the third cathode patterns (R, G, B) respectively. The reason for combining is same as claim 1.

**Regarding claim 4,** Urabe discloses a partition rib structure (6) disposed over the active device matrix and the anode pattern layer (fig 4C, active device matrix is below anode A), and the first, the second, and the third organic pattern are isolated from each other (figs 3, 4C).

**Regarding claim 5,** Urabe discloses the partition rib structure (6) isolates the first, the second, and the third cathode pattern (figs 3, 4C).

**Regarding claim 7,** Urabe discloses the first, the second, and the third organic pattern are RGB (fig 3).

**Regarding claim 8,** Urabe discloses the active device matrix comprises TFT array (figs 5 and 6).

**Regarding claim 21,** Yuki discloses the first cathode pattern (figure 7, R) is electrically connected to the first voltage (701) through the first cathode line (704), the second cathode pattern (figure 7, G) is electrically connected to the second voltage (702) through the first cathode line (705), and the third cathode pattern (figure 7, B) is electrically connected to the third voltage (703) through the first cathode line (706). The reason for combining is same as claim 1.

**Regarding claim 22,** Yuki discloses in the figure 7, the first, second, and third cathode patterns (R, G, B) extend alone a first direction (top to bottom or vice versa), and the first, second, and third cathode lines (704, 705, 706) extend alone a second direction

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different from the first direction (left to right or vice versa). The reason for combining is same as claim 1.

**Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Urabe in view of Yuki, in further view of Fery (2004/0075115).**

Urabe in view of Yuki discloses all the claimed limitations except for the partition rib structure has width of the top surface being greater than width of the bottom surface.

Fery discloses an OLED (fig 2) having a partition rib structure (105) that isolates cathodes (103) as well as organic layers (102), and has width of the top surface being greater than width of the bottom surface (fig 2), for the purpose of effectively separating the cathodes and organic layers.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a partition rib structure has width of the top surface being greater than width of the bottom surface disclosed by Fery in the OLED panel disclosed by Urabe in view of Yuki, for the purpose of effectively separating the cathodes and organic layers.

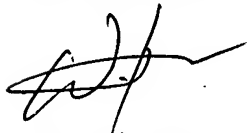
***Contact information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bumsuk Won whose telephone number is 571-272-2713. The examiner can normally be reached on Monday through Friday, 8:00 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar Patel can be reached on 571-272-2457. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Bumsuk Won  
Patent Examiner



JOSEPH WILLIAMS  
PRIMARY EXAMINER